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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,610	12/29/2000	William A. Harris	H16-26054 US	8597
128	7590	04/28/2005	EXAMINER	
HONEYWELL INTERNATIONAL INC.			LAM, TUAN THIEU	
101 COLUMBIA ROAD				
P O BOX 2245			ART UNIT	
MORRISTOWN, NJ 07962-2245			2816	
			PAPER NUMBER	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

Office Action Summary	Application No. 09/751,610	Applicant(s) HARRIS, WILLIAM A.	
	Examiner Tuan T. Lam	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,20-24,26-29,31-37,39-45,47 and 48 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,20-24,26-29,31-37,39-45,47 and 48 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/2/2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/17/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a response to the amendment filed 3/17/2005. Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 are pending and are under examination.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 10, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered and a signed copy of the IDS has mailed to the applicant on 3/10/2005. Another signed copy of the IDS is provided along with this Office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 are rejected under 35 USC 103(a) as being unpatentable over Li (USP 5,058,132) in view of Epstein (USP 4,093,870), both prior art of record, and Mano (Computer Engineering Hardware Design, 1988, pages 130-132), newly cited reference.

Figure 2 of Li shows a circuit for dividing an input clock signal into N clock signals having a relative phase separating of $360/2N$, where N (N is 5, column 5, lines 50-64) is a positive integer, the circuit comprising: a phase locked loop (102) receiving an input signal (116) having a frequency F0 (125 Mhz) and providing an output signal (signal 124 having a signal of $2NF_0 = 12.5$ Mhz) having a frequency of $2NF_0$, a Johnson counter (114) having N stages (5 flip

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flops, column 5, lines 50-64) connected to receive as an input the output signal (124) of the phase locked loop circuit (102) and providing an output signal (LBC1-5) as an error signal to the phase locked loop circuit (column 5, lines 25-28), and the Johnson counter (114), having at least 5 flip flop circuits (stages), also connected for providing at least two output signals (LBC1-5) from at least two of the N stages of the Johnson counter (114) as clock signals each having a phase displaced from the phase of the other $360/2N$ degrees.

Li reference does not disclose the Johnson counter (114) having N JK flip flops with the particular arrangement as called for in claims 1, 20, 32 and 40. Epstein's figure 4 discloses a Johnson counter using JK flip flops with a particular arrangement as claimed. Mano's reference further teaches that JK flip flop is reliable because it does not have the undermined states (page 131, third paragraph). Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to implement the 5 stages (flip flop circuits) Johnson counter of Li with a five JK flip flop circuit arranged as in Epstein because JK flip flop is reliable thus preventing the counter from erroneous operation as taught by Mano.

Regarding claims 2-3, 21, 33-34, 41-42 and 48, the combination of Li, Epstein and Mano references discloses N is 5. However, depending on the frequency of the input signal, the output frequency of the VCO can be divided up or down (N=4 required in claims 2, 21, 33 and 41; N=8 required in claims 3, 34, 42 and 48) to be in synchronized with the input signal without changing the overall operation of the circuit. Thus, the dividend factor N is a design expedient dependent on the particular application. Therefore, the limitation of using N equals 4 or 8 as recited in claims 2, 21 and 3 will not be patentable under 35USC 103(a).

Regarding claim 22, each signal LBC1-5 has a frequency of $2NF_0$.

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Regarding claims 23 and 35-36, the error signal (output of the VCO of Li) has a frequency equal to F_0 .

Regarding claims 24, 29, 37 and 45, Li shows a phase detection (104), low pass filter and gain stage (106) and VCO (108).

Regarding claims 26, 31, 39 and 47, each Q output and complementary Q output of each JK flip flop is coupled to provide a clock signal, the $2N$ clock signals having relative phase separation of $360/2N$ degree, and each clock signal having a frequency F_0 .

Regarding claims 27 and 43-44, the feedback signal is seen as the feedback in (123) of Li reference.

Regarding claim 28, each clock output has a frequency F_0 .

Response to Arguments

Applicant's arguments filed 3/15/2005 have been fully considered but they are not persuasive.

Applicant argues that the combination of Li (USP 5,058,132), Epstein (USP 4,093,870) and Mano references does not show a Johnson counter comprising an input JK flip flop, an output JK flip flop, and a plurality of middle JK flip flops as called for in the independent claims 1, 20, 32 and 40 is not persuasive. As noted above under the 35USC 103(a) section, Li reference shows a Johnson counter (114) having a plurality of stages but does not disclose the Johnson counter having N JK flip flops with the particular arrangement as called for in claims 1, 20, 32 and 40. Epstein's figure 4 discloses a Johnson counter using JK flip flops with a particular arrangement as claimed. Mano's reference further teaches that JK flip flop is reliable because it does not have the undermined states (page 131, third paragraph). Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to implement the 5 stages (flip flop

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circuits) Johnson counter of Li with a five JK flip flop circuit arranged as in Epstein because JK flip flop is reliable thus preventing the counter from erroneous operation as taught by Mano.

The Examiner has clearly presented evidences and motivation as how the prior art references are combined in compliance with MPEP. Therefore, claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 remain rejected under 35USC 103(a).

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Tuan T. Lam', with a long horizontal flourish extending to the right.

Tuan T. Lam
Primary Examiner
Art Unit 2816

4/26/2005